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**PATENT APPLICATION (NG)**

**RESPONSE UNDER 37 CFR §1.116  
EXPEDITED PROCEDURE  
TECHNOLOGY CENTER ART UNIT 3723**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Makoto KOBAYASHI et al.

Group Art Unit: 3723

Application No.: 09/830,434

Examiner: H. Shakeri

Filed: April 26, 2001

Docket No.: 109352

For: POLISHING PAD AND POLISHING METHOD FOR SEMICONDUCTOR WAFER

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**AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116**

Director of the U.S. Patent and Trademark Office  
Washington, D.C. 20231

RECEIVED

OCT 29 2002

TECHNOLOGY CENTER R3723

Sir:

In reply to the July 26, 2002 Office Action, please amend the above-identified

application as follows:

**IN THE CLAIMS:**

Please replace claims 11-13, 17, 18, 20, 21 and 27-31 as follows:

*Subj 17*  
11. (Amended) A polishing pad used for polishing a semiconductor wafer in a mirror polishing process, wherein a content of zinc oxide (ZnO) included in the polishing pad is 200ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.

*CJ*  
12. (Amended) A polishing pad used for polishing a semiconductor wafer in a finish polishing process, wherein a content of zinc oxide (ZnO) included in the polishing pad is 100ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.

13. (Amended) A polishing pad used for polishing a semiconductor wafer in a finish polishing, wherein the polishing pad does not include zinc oxide (ZnO).